Owuraku Dompreh

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Education

University of Warwick — Coventry, England
MEng in Computer Systems Engineering — *Sep. 2025 – Present*

- **Relevant Modules:** Computer Organisation & Architecture, Electrical & Electronic Circuits, Systems Modelling & Simulation

Engineering Projects

Real-Time Deterministic Control System (Bare-Metal C++) | *C++, avr-gcc, Python*

- **Architected** a modular **2,000+ LOC** bare-metal firmware stack (**avr-gcc**), decoupling hardware abstraction, state estimation, and control logic to model the low-latency requirements of complex physical systems.
- **Developed** a custom Hardware Abstraction Layer (**HAL**) bypassing standard frameworks; utilised direct memory-mapped I/O, bitwise register manipulation, and a Serial Peripheral Interface (**SPI**) to drive multiplexed I/O via a 74HC595 shift register with **microsecond-level latency**.
- **Engineered** a deterministic, cooperative scheduler using hardware timer interrupts (**ISRs**) to manage a 6-state Finite State Machine (**FSM**), eliminating Real-Time Operating System (**RTOS**) overhead and achieving real-time constraints.
- **Implemented** closed-loop Proportional-Integral-Derivative (**PID**) control utilising fixed-point arithmetic to bypass missing FPU limitations, fusing non-blocking Analog-to-Digital Converter (**ADC**) reads and Timer-based input captures from 4 sensors to track setpoints and reject injected noise.
- **Analysed** .elf binaries via avr-objdump to optimise assembly efficiency for a **2 kHz** control loop; streamed custom UART telemetry to **Python** for live PID tuning.

Research Project – Algorithmic System Modelling | *Python, PennyLane*

- **Engineered** high-performance simulation workflows using **Python** and **PennyLane** (leveraging its **C++** backend) to evaluate Parametrised Quantum Circuits (**PQCs**) for generative data sampling.
- **Optimised** quantum circuit architectures to bypass severe computational bottlenecks found in deep **40+ layer** algorithms, mitigating barren plateaus to drastically reduce simulation overhead and parameter training time.
- **Benchmarked** hardware execution limits and resource scaling, successfully mapping complex mathematical models into hardware-efficient gate sequences while achieving a Mean Squared Error (**MSE**) convergence of **1.8e-3**.

Work Experience

Machine Learning Intern — Summer 2026
Warwick Manufacturing Group — *Coventry, England*

- **Architected** a hybrid hardware-software integration framework in **Python**, mapping data transfer pathways between classical infrastructure and the Quantum Approximate Optimisation Algorithm (**QAOA**).
- **Engineered** simulation pipelines to compile high-dimensional datasets into quantum circuits, explicitly optimising gate depth to meet the strict physical limits of Noisy Intermediate-Scale Quantum (**NISQ**) hardware.
- **Profiled** computational resource scaling against classical solvers, quantifying system-level trade-offs in gate error rates and projecting an **18% reduction** in total execution latency.

Technical Skills

Languages: C, C++, Python, MATLAB, Bash, Assembly
Embedded Systems: AVR Microcontrollers, I2C, SPI, UART, Hardware Timers, Interrupts (ISR)
Systems Engineering: PID Control, FSM, Telemetry Logging
Tools and Equipment: PlatformIO, Git, Oscilloscopes, Logic Analysers, Multimeters